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A MICRON-THICKNESS, PLANAR SCHOTTKY DIODE CHIP FOR TERAHERTZ APPLICATIONS WITH THEORETICAL MINIMUM PARASITIC CAPACITANCE

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Abstract

The design and fabrication of a novel planar Schottky diode with greatly reduced shunt capacitance for millimeter and submillimeter wave applications is described. The dominant pad-to-pad shunt capacitance is minimized by replacing the substrate GaAs with a low-dielectric substitute. This replacement substrate can be easily removed by the user after the device is soldered into the mixer circuit. This will yield minimum possible pad-to-pad shunt capacitance.

I. Introduction

Whisker-contacted Schottky barrier diodes on gallium arsenide have been the device of choice for millimeter and submillimeter wavelength heterodyne receivers for many years. This simple structure enables the production of very small area devices with low junction capacitance and extremely low parasitic shunt capacitance [1,2]. Although Superconductor-Insulator-Superconductor (SIS) junctions are replacing diodes in millimeter wavelength applications which require the greatest possible sensitivity, operation in the submillimeter wavelength range has not been realized. Also, many applications require mixer operation in the 77 to 300 K temperature range, which is not possible with current SIS materials.

Planar, whiskerless Schottky diodes have been fabricated by this and other laboratories, and commercial monolithic diodes are available for application at frequencies up to about 100 GHz. Planar structures offer ruggedness and ease of use compared to whisker-contacted diodes and open the door to integrated circuit designs. The limitations on frequency response and conversion loss are related primarily to the difficulty in producing micron and submicron anode diameters and the inherently higher shunt capacitance of the planar structures. The focus of this work is the design and fabrication of a new planar diode structure which offers greatly reduced shunt capacitance. The key element of this design is the replacement of the normal gallium arsenide substrate of the chip with quartz or the complete removal of the supporting substrate. This results in the lowest possible shunt capacitance without sacrificing the desirable characteristics of the planar diode configuration.

The basic structure of the planar Schottky diode is discussed in section II. Although this structure holds great promise, the difficulty of fabrication and the inherently higher shunt capacitance has limited its usefulness. In section III we review the surface channel diode that has been developed at UVa. This novel surface channel technology allows critical fabrication steps to be done on a planar surface. In section IV pad-to-pad capacitance is shown to be the principal source of parasitic shunt capacitance and elimination of the high dielectric substrate is shown to be a viable solution to this problem. Our technique for removing the substrate is outlined in section V. A discussion of the implications of this new diode technology is presented in section VI, and a brief conclusion is given in section VII.

II. Planar Diode Structure

A cross section of a hypothetical mesa diode is shown in Fig. 1. It consists of anode and cathode (ohmic) contact pads of sufficient size for bonding, a narrow anode contact finger which bridges between the anode pad and the Schottky junction, conductive material between the Schottky diode and the ohmic contact, and an insulating substrate to support the structure. Shown in phantom view are the two major shunt capacitance elements, the parallel plate capacitance of the finger overlying GaAs, and the pad-to-pad capacitance due to fringing field lines through the substrate dielectric. The pad-to-pad capacitance is by far the dominant capacitance in present chip designs.

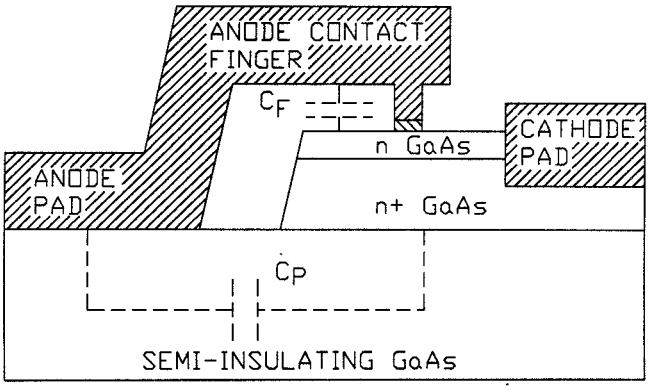


Figure 1. Cross Sectional View of a Typical Mesa Diode

Contact finger capacitance can be minimized by reducing the finger area overlying the active layer, increasing the separation between the finger and underlying conductive material, or decreasing the dielectric constant of intervening material. Pad-to-pad capacitance can be reduced by reducing pad area, increasing pad separation, reducing the substrate dielectric constant, or reducing the thickness of the substrate. However, pad and finger area and separation are constrained by practical considerations. Finger width cannot be reduced to the point of producing problems with resistance, physical strength or lithographic alignment. Pad dimensions are limited by considerations of handling and bonding and by ohmic contact resistivity. Also, large pad spacing is undesireable since this would lead to excessive inductance from the long, narrow contact finger. Thus the only viable method to reduce the shunt capacitance significantly is to alter the chip substrate.

III. Surface Channel Diode

The surface channel planar diode, as fabricated at the University of Virginia, is shown in Fig. 2 [3,4]. In this structure, a trench is etched across the width of the chip and completely under the anode contact finger. This channel isolates the anode contact pad from the diode junction and eliminates the need for a mesa. It is formed near the end of the fabrication sequence, after the anode contact finger is fabricated. Advantages of this structure compared to a mesa design include:

1) Planar wafer surface during the critical steps of anode definition and alignment of the contact finger to the anode.

2) Contact finger air bridge which provides a large (5 micron) gap between the finger and the underlying semi-insulating GaAs for most of its length. The finger overlies conductive GaAs (with intervening SiO_2 dielectric) only over approximately 2 to 4 microns, depending on the specific design. This SiO_2 can be removed for reduced capacitance.

3) Smaller finger inductance per unit of finger capacitance due to the straight line configuration (i.e., the finger does not need to follow the contours of a mesa). A wide range of finger lengths (5 to 50 microns) and widths can be easily fabricated.

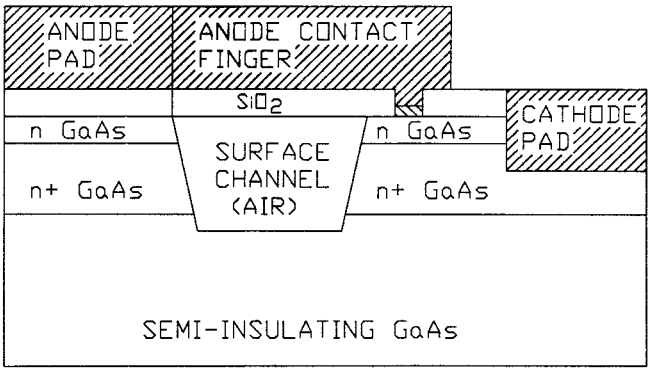


Figure 2. Cross Sectional View of the UVa Surface Channel Diode

This device has been used successfully in applications up to 183 GHz. However, the performance is limited by the large shunt capacitance from the pads and the adverse effect of the high dielectric substrate on the propagation of the RF signal near the diode.

IV. Anode-to-Cathode Pad Shunt Capacitance

To examine the magnitude of the pad-to-pad capacitance and the effect of substrate thickness, a large scale model was constructed from sheets of Transtech D-13 ceramic dielectric. This material has a relative dielectric constant of 13. Each piece was 4 x 4 x 1/4 inches with a surface finish of 10 microinches. Copper foil pads, 1-3/4 x 4 inches were applied to the face of one sheet to represent the anode and cathode pads of the planar diode. Capacitance between the pads was measured by contacting the pads with probes made from lengths of semiridgid coaxial tubing connected to an HP 4275A LCR meter. A small section of the center conductor extended beyond the shield to serve as a probe contact. The graph in Fig. 3 gives capacitance versus substrate thickness. When scaled by a factor of 800, this data predicts a pad-to-pad capacitance of 13.4 fF for a chip which is 5 x 5 x 5 mils with 5 x 2.2 mil pads spaced 0.6 mils apart. Reducing thickness only marginally reduces capacitance unless the chip is made very thin compared to its width or length.

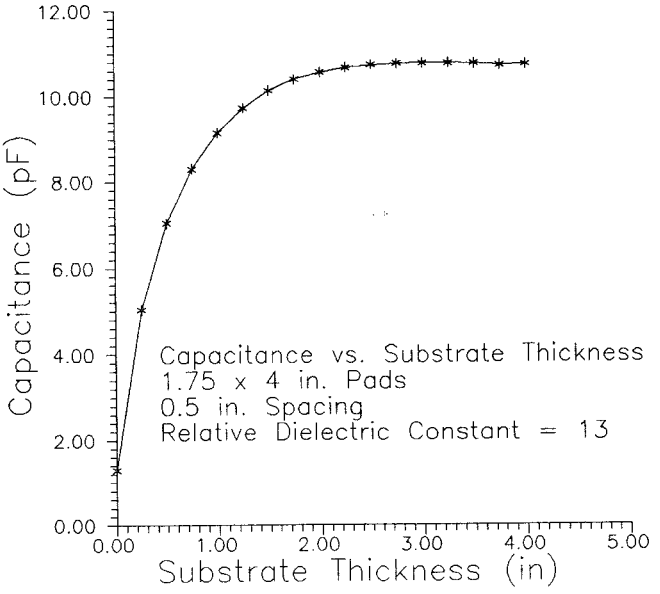


Figure 3. Pad-to-Pad Capacitance vs. Substrate Thickness for a Generic Planar Diode Structure

Pad capacitance can, of course, also be reduced by decreasing pad area and/or increasing pad separation. However, this is is not always a practical solution (see section 11). The smallest feasible chip design will have anode and cathode pads 2 x 2 mils spaced 2 mils apart on a 2 mil insulating substrate. A 500X scale model (ε_r=13) has indicated that this structure will have a shunt capacitance of 3 fF. This shunt capacitance is approximately six times the junction capacitance of whisker-contacted diodes currently fabricated at the University of Virginia used for operation in the 1 - 3 THz range [1]. This does not include contributions from the anode contact finger.

The various planar diode structures, including mesa, proton isolated and surface channel designs, have essentially the same pad-to-pad shunt capacitance for the same pad size and spacing. All three can be fabricated to include air bridge anode contact fingers to reduce the shunt capacitance of the finger. One must be very careful in the evaluation of measured or estimated values of planar diode parasitic capacitance. For example, some researchers have fabricated mesa diodes with total parasitic capacitance values estimated to be less than one fF [5]. From the results given above, this is possible only if the pad-to-pad capacitance is neglected. Although this may be justifiable in cases where the pads are part of the microwave circuit, in general the high dielectric substrate will degrade the coupling of the RF signal into the diode. For this reason we prefer to directly measure the total "free space" capacitance of the chip. This conservative value is the worst case and the user's embedding circuit may serve to reduce the effect of this capacitance.

V. Elimination of High Dielectric Substrate

Shunt capacitance from the contact pads and, to a degree, from the contact finger, can be greatly reduced by removing the GaAs substrate completely or by replacing it with a material of lower dielectric constant. Either of these alternatives can be easily implemented in the surface channel diode with the inclusion of an etch stop layer between the substrate GaAs and the n+ buffer layer as shown in Fig. 4. Structures with AlGaAs layers and high quality GaAs active layers are easily produced at low cost by OMVPE techniques. The surface channel diode fabrication sequence is carried out using procedures described elsewhere. The surface channnel is etched slightly (0.5 um) into the AlGaAs layer with a wet chemical etch which is not selective for AlGaAs over GaAs.

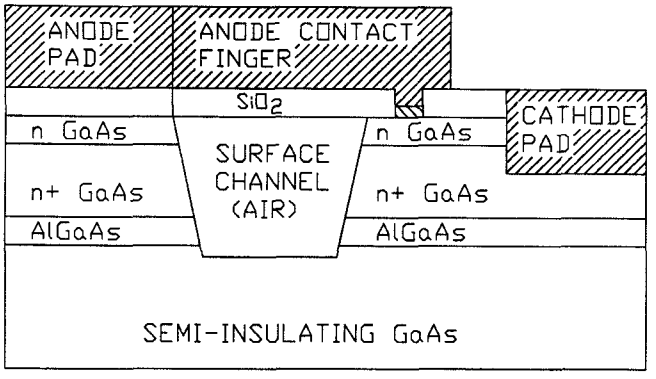
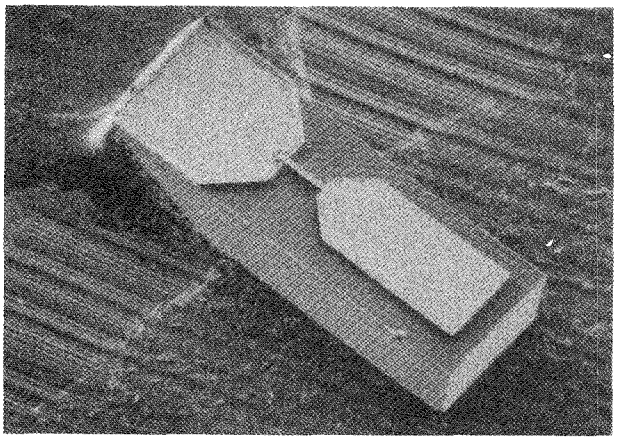
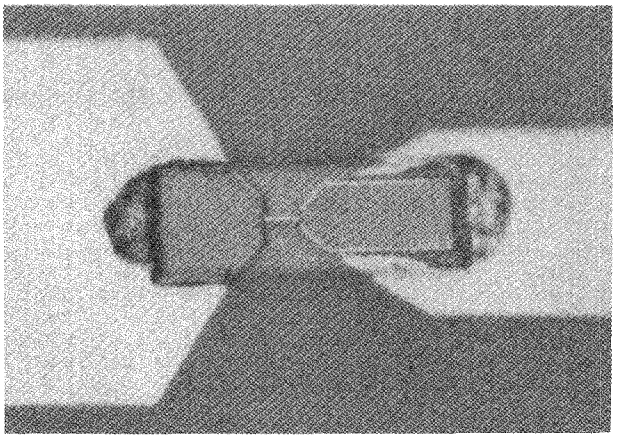


Figure 4. Cross Sectional View of the Surface Channel Diode with AlGaAs Etch Stop Layer



(a)



(b)

Figure 5. Surface Channel Diodes with Quartz Substrate Before Soldering (Above) and After Soldering to a Stripline (Below)

Our first attempt to remove the GaAs substrate was carried out on individual chips after first soldering or bonding the chip to the RF circuit. The edges and the surface channel region of the mounted chip were masked with an organic polymer and the GaAs was etched away with a wet chemical etchant which stopped at the AlGaAs layer. This method is effective although somewhat tedious. The resulting I-V characteristic is identical to that of the original chip.

A second option is to continue processing the wafer on the backside to remove the GaAs substrate and replace it with a suitable substitute which will serve as a permanent or easily removable substrate at the chip level. A fabrication sequence has been developed to accomplish this goal. After the normal surface channel fabrication is carried out, the wafer is bonded to a carrier slice using a material(s), A1, which fills the surface channel. The substrate GaAs is removed down to the AlGaAs etch stop layer with a selective wet chemical etchant. Optionally, the AlGaAs is then etched until it is completely removed. Next, a thin (2 mil) piece of quartz is bonded to the exposed epitaxial layers using an appropriate adhesive, A2. The wafer is then diced from the backside to separate the individual chips. Alignment for dicing is done visually through the quartz substrate. The resulting chips are finally released from the carrier slice by dissolving the bonding/filling agent, A1, in an appropriate solvent. Obviously, this solvent must not attack A2. Adhesive A2 may be a permanent type, such as epoxy, or it may be a polymer which is easily removable. Experimental fabrication trials have produced diced chips with GaAs epitaxial layers bonded to 2 mil quartz with very smooth egdes on both front and back surfaces. Chips as small as 2 x 6 x 2 mils thick have been produced.

A surface channel diode chip with a quartz substrate is shown in Fig. 5. In Fig. 5a the chip is shown before soldering and in 5b the chip is shown after soldering to a stripline. The diode features are visible through the quartz substrate. The chips are 5 x 15 x 3 mils thick with a 50 micron anode contact finger. The striking feature is the tranparency of the substrate. In a priliminary test of the physical integrity of this structure, a quartz substrate chip was immersed in liquid nitrogen and then allowed to return to rooom temperature. This was repeated five times with no change in the I-V characteristic.

The quartz-to-epi bond for the chips shown in Fig. 5 is made with an adhesive which is easily removed with a selective solvent which does not attack GaAs, silicon dioxide, quartz or most metals. The chips with quartz substrate can be easily handled with tweezers or vacuum tools to facilitate bonding to the microwave circuit in a flip-chip manner. The transparent substrate can be a very useful aid in positioning the chip with respect to the anode. Once bonded, the quartz substrate can be left in place or may be removed for absolute minimum shunt capacitance. An SEM photograph of a substrateless diode chip is shown in Fig. 6. The total thickness of this device, exclusive of the solder pads, is approximately 6 microns. This includes pad metallization (gold plate), oxide layer, and epitaxial GaAs. The bonding pads are connected only by the contact finger. In this case virtually all of the pad-to-pad capacitance can be considered to be part of the planar transmission line leading to the diode.

These prototype devices have demonstrated the feasability of replacing the GaAs substrate with a material of reduced dielectric constant or the complete removal of the GaAs in a mounted chip. Work in underway to optimize the fabrication procedure and to fabricate devices which are optimized for submillimeter wavelength applications.

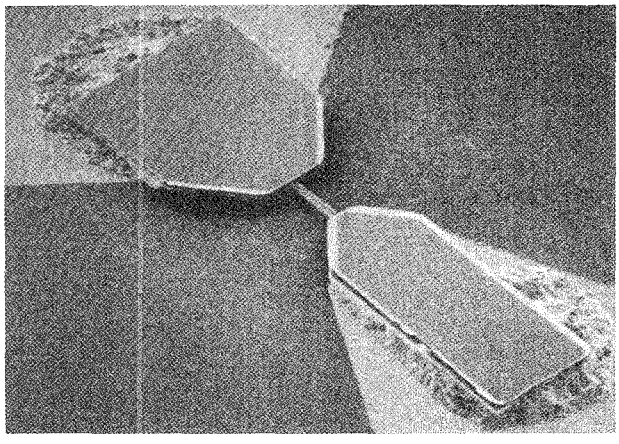


Figure 6. Surface Channel Diode on Microstrip with Substrate Removed

VI. Implications for Millimeter and Submillimeter Wavelength Devices

The quartz substrate and substrateless planar Schottky diode structures will be most effective in improving millimeter and submillimeter wavelength hybrid circuit receiver performance. Both waveguide and quasi-optical designs will benefit from the low shunt capacitance and also from the very minimal discontinuity presented by the substrateless diode. If the anode and cathode pads are extended to form an integral planar antenna such as a bow-tie or log periodic type, energy can be coupled through the quartz substrate. This quartz can be Z-axis crystalline for excellent transmission and the thickness can be chosen for optimal coupling at a particular wavelength.

There are also many variations on the concept of substrate replacement or removal, in terms of fabrication and device applications. Integrated circuits could be produced on quartz as well as discrete devices. Some other dielectric (spin-on glass, sputtered SiO_2, polyimid, etc.) could be deposited by varied means in place of adhesive-bonded quartz. The original GaAs substrate or the replacement substrate could be patterened and etched in selective areas to form isolated regions which are left in membrane form or filled in with other materials.

It is conceivable, and we believe very realistic, that photolithography and other processes can be performed on the backside of the epilayer, while the wafer is still attached to the carrier slice. For example, unwanted epitaxial GaAs could be removed, exposing the underlying metallization. This may be very important for integral antenna designs. Backside processing on the replacement substrate could also be performed after attaching it to the epitaxial layer. This would facilitate via hole formation and backside metalization. Alignment to frontside features would be simplified by the transparent substrate.

VII. Conclusions

A fabrication process has been developed which replaces the GaAs substrate of discrete devices or integrated circuits with a low dielectric constant material (e.g., quartz) which may be permanent or easily removable. Minimum possible shunt capacitance results when the substrate is removed after bonding the device to the RF circuit. The substrateless diode will also minimize the disturbance of radiation patterns in waveguides and quasi-optical mixers. The process has wide implications for integrated diode-antenna receivers and MMIC applications. This technology combined with reduced anode diameter and optimal fabrication materials and techniques will result in reduced conversion loss and improved sensitivity in Schottky diode receivers at millimeter and submillimeter wavelengths.

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